

What is claimed is:

- 1 1. A method of manufacturing an integrated circuit package, comprising:
2 providing a substrate comprising:
3 a first surface,
4 a second surface opposite said first surface,
5 a cavity through said substrate between said first and second
6 surfaces, and
7 a conductive via extending through said substrate and electrically
8 connecting said first surface of said substrate with said second surface of said substrate;
9 applying a strip to said second surface of said substrate;
10 mounting a semiconductor die on said strip, at least a portion of said
11 semiconductor die being disposed inside said cavity;
12 encapsulating in a molding material at least a portion of said first surface
13 of said substrate; and
14 removing said strip from said substrate.
- 1 2. The method of claim 1, said encapsulating further comprising filling said
2 cavity with said molding material, wherein a surface of said semiconductor die is exposed
3 to said strip.
- 1 3. The method of claim 2, further comprising attaching a thermal element to
2 said exposed surface of said semiconductor die.
- 1 4. The method of claim 3, said attaching said thermal element comprising
2 bonding a thermally conductive adhesive to said thermal element.

1 5. The method of claim 4, said attaching said thermal element further
2 comprising attaching said thermal element to said second surface of said substrate.

1 6. The method of claim 1, said mounting said semiconductor die comprising
2 disposing said die in its entirety inside said cavity.

1 7. The method of claim 3, said thermal element comprising a copper heat
2 slug.

1 8. The method of claim 1, said substrate further comprising a multi-layer
2 circuit trace.

1 9. The method of claim 1, further comprising, after said mounting said
2 semiconductor die on said strip, interconnecting said semiconductor die to a first trace
3 embedded in said first surface of said substrate.

1 10. The method of claim 9, said interconnecting comprising a thermo-sonic
2 wire bonding process.

1 11. The method of claim 1, said encapsulating comprising a liquid molding
2 process.

1 12. The method of claim 1, said encapsulating comprising a transfer molding
2 process.

1 13. The method of claim 1, said encapsulating comprising encapsulating said
2 first surface of said substrate in its entirety.

1 14. The method of claim 1, further comprising attaching a solder element to a
2 second trace embedded in said second surface of said substrate.

1 15. The method of claim 1, said applying said strip comprising applying an
2 adhesive material on at least a portion of said strip to said second surface of said
3 substrate.

1 16. The method of claim 15, said strip comprising a high temperature stable
2 polyimide.

1 17. The method of claim 15, said mounting said semiconductor die
2 comprising attaching said semiconductor die to said adhesive material on said strip.

1 18. The method of claim 1, said applying said strip further comprising sealing
2 a portion of said cavity.

1 19. A method of manufacturing an integrated circuit package, comprising:
2 providing a substrate comprising:

3 a first surface,

4 a second surface opposite said first surface,

5 a plurality of cavities, each said cavity through said substrate

6 between said first and second surfaces, and

7 a plurality of conductive vias, each said via extending through said

8 substrate and electrically connecting said first surface of said substrate with said second

9 surface of said substrate;

10 applying a strip to said second surface of said substrate;

11 mounting a plurality of semiconductor dies on said strip, at least a portion

12 of each said semiconductor die being disposed inside each said cavity;

13 encapsulating in a molding material at least a portion of said first surface

14 of said substrate; and

15 removing said strip from said substrate to expose a surface of each said
16 semiconductor die.

1 20. The method of claim 19, further comprising singulating said substrate into
2 a plurality of integrated circuit packages.

1 21. The method of claim 20, said singulating comprising a sawing process.

1 22. The method of claim 20, said singulating comprising a punching process.

1 23. An integrated circuit package comprising:
2 a substrate comprising:

3 a first surface,

4 a second surface opposite said first surface,

5 a cavity through said substrate between said first and second
6 surfaces, and

7 a conductive via extending through said substrate and electrically
8 connecting said first surface of said substrate with said second surface of said substrate;

9 a semiconductor die electrically coupled with said conductive via, at least
10 a portion of said semiconductor die being disposed inside said cavity of said substrate;

11 an encapsulant material encapsulating a portion of said semiconductor die
12 such that at least a portion of a surface of said semiconductor die is exposed.

1 24. The integrated circuit package of claim 23, further comprising a
2 conductive member adapted for attachment of said integrated circuit package to an
3 external device.

1 25. The integrated circuit package of claim 24, said conductive member
2 attached to said second surface of said substrate.

1 26. The integrated circuit package of claim 23, further comprising at least one
2 wire electrically coupling said semiconductor die with said conductive via.

1 27. The integrated circuit package of claim 23, at least a portion of said first
2 surface of said substrate being adapted for coupling said integrated circuit package with a
3 second integrated circuit package.

1 28. The integrated circuit package of claim 23, said substrate further
2 comprising a multi-layer trace embedded therein.

1 29. An integrated circuit package assembly comprising the integrated circuit
2 package of claim 23 attached to at least one other integrated circuit package.

1 30. The integrated circuit package assembly of claim 29, wherein one of said
2 integrated circuit packages is stacked on top of at least one of the other of said integrated
3 circuit packages.

1 31. The integrated circuit package assembly of claim 29, further comprising a
2 heat slug thermally coupled with at least one of said integrated circuit packages.

1 32. The integrated circuit package of claim 23, said package having a
2 thickness dimension of about one millimeter.

1 33. The integrated circuit package of claim 32, said package having a width
2 dimension of about seven millimeters.

1 34. The integrated circuit package of claim 23, said substrate being
2 substantially planar and said semiconductor die being aligned in a plane with said
3 substrate.

1 35. The integrated circuit package of claim 23, said integrated circuit package
2 being a land grid array.

1 36. The integrated circuit package of claim 23 said integrated circuit package
2 being a ball grid array.

1 37. The integrated circuit package of claim 23, said encapsulant material
2 comprising an epoxy.

1 38. The integrated circuit package of claim 23, further comprising a ring-like
2 trace embedded in said substrate.

2025-05-01 10:00:00